NIT-201-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Accompanying Divisional Application under 37 CFR 1.53:

Prior Application: N. KATOH et al
Serial No. 09/582,327
Filed: June 23, 2000

Group Art Unit: 2819
Examiner: A. Tran
For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, STORAGE MEDIUM ON WHICH CELL LIBRARY IS STORED AND DESIGNING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above application as follows.

IN THE CLAIMS

Please rewrite claims 22 and 23 as set forth below.

22. (Amended) A designing method for a semiconductor integrated circuit device according to claim 21, using the storage medium on which there is stored the cell library, comprising at least the steps of:

calculating consumption power and a delay of a signal path; and

assigning to a logic circuit one cell selected among at least two kinds of cells constructed of switching elements which have different threshold voltages while having the same function and the same shape, using the result of the step of calculating consumption power and a delay of a signal path.

23. (Amended) A designing method for a semiconductor integrated circuit according to claim 21, using the storage medium on which there is stored the cell library, comprising at least the steps of:

designing a logic circuit using only cells constructed of switching elements each with a high threshold value;

calculating consumption power and a delay of a signal path; and

replacing a part of the logic circuit designed using only cells constructed of switching elements each with a high threshold value, by a cell constructed of switching elements each of which has a low threshold value while having the same function and the same size.

REMARKS

Examination is respectfully requested.

Respectfully submitted,

30,293

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Date: February 28, 2002

MARKED UP VERSION OF REWRITTEN CLAIMS

22. (Amended) A designing method for a semiconductor integrated circuit device according to [any one of claims 1 to 20] claim 21, using the storage medium on which there is stored the cell library [according to claim 21], comprising at least the steps of:

calculating consumption power and a delay of a signal path; and

assigning to a logic circuit one cell selected among at least two kinds of cells constructed of switching elements which have different threshold voltages while having the same function and the same shape, using the result of the step of calculating consumption power and a delay of a signal path.

23. (Amended) A designing method for a semiconductor integrated circuit according to [any of claims 1 to 20] claim 21, using the storage medium on which there is stored the cell library [according to claim 21], comprising at least the steps of:

designing a logic circuit using only cells constructed of switching elements each with a high threshold value;

calculating consumption power and a delay of a signal path; and

replacing a part of the logic circuit designed using only cells constructed of switching elements each with a high threshold value, by a cell constructed of switching elements each of which has a low threshold value while having the same function and the same size.